ABSTRACT OF THE DISCLOSURE

A power management system for digital circuitry uses data buffer monitoring to determine appropriate processor clock speed or voltage. This allows a processor to be switched from a low power state to a high power state when a monitored data buffer level feeding data to a power intensive application is greater than a second memory buffer level. The processor is switched from a high power state to a low power state when the monitored data buffer level is less than a first memory buffer level.